REMARKS

Claims 1-8, 10-13 and 23-38 are all the claims presently pending in the application.

Claim 11 stands rejected upon informalities (e.g., 35 U.S.C. § 112, second paragraph), and claims 1-8, 10-13, and 23-38 stand rejected on prior art grounds.

With respect to the prior art rejections, claims 1, 4, 10, 25, and 26 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 24 and 28-31 of Ajmera et al. (U.S. Patent No. 6,503,833 B1). Claims 1, 4, 10, 25, and 26 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over

Additionally, claims 1, 10 and 16 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 24 and 28-31 of Ajmera (U.S. Patent No. 6,503,833 B1), provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 24 and 28-31 of Application No. 10/287,476, rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 27 of Cabral Jr., et al., (U.S. Patent No. 6,444,578 B1), provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 4, 5, and 23 of Application No. 10/299,688, and provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15 and 20 of 09/569,306.

Further, claims 1-6, 8, 10-13, and 23-38 stand rejected under 35 U.S.C. § 103 as being unpatentable over anticipated by Maa et al. (U.S. Patent No. 5,830,775 in view of Cabral, Jr., et al. (U.S. Patent No. 5,828,131).

These rejections are respectfully traversed in view of the following discussion.

It is noted that the claim amendments herein are made only for more particularly pointing out the invention for the Examiner, and not necessarily for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

Further, it is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution. Thus, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

I. THE CLAIMED INVENTION

Applicant's invention, as exemplarily disclosed and claimed (e.g., see independent claim 1), is directed to a method for fabricating a silicide for a semiconductor device, which includes depositing a metal containing silicon on a silicon substrate, reacting the metal containing silicon to form a first silicide phase, etching any unreacted metal containing silicon, depositing a silicon cap layer over the first silicide phase, reacting the silicon cap layer to form a second silicide phase, for the semiconductor device, and etching any unreacted silicon from the silicon cap layer.

Independent claims 4, 10, 13, 25, and 26 recite somewhat similar methods, but with some different limitations.

With such features and as mentioned previously, a reaction of a metal (e.g., Co in an exemplary embodiment, but other metals will be similarly operable as claimed and as clearly described in the specification) containing silicon, to initially form Co_2Si, minimizes the silicon consumption of the thin SOI film (or bulk silicon) substrate.

The consumption of the thin SOI film is additionally reduced by the deposition of a silicon (or poly-silicon in a non-limiting exemplary variation of the invention) film on the Co_2Si.

Such exemplary features are not taught or suggested by any other prior art of record, either alone or in combination.

II. THE 35 U.S.C. §112, SECOND PARAGRAPH, REJECTION

While Applicant submits that the claims are clear to one of ordinary skill in the art to recognize the metes and bounds of the invention, to speed prosecution, claim 11 has been amended in a manner believed fully responsive to the Examiner's criticisms.

Thus, claim 11 is believed to be clear and sufficiently definite to one of ordinary skill in the art to know the metes and bounds of the invention.

In view of the foregoing, reconsideration and withdrawal of this rejection are respectfully requested.

III. THE PRIOR ART REJECTIONS

A. The §103(c) Rejection Based on Maa et al. In View of Cabral et al. '131

Maa et al. (and all of its deficiencies) has been discussed in the November 24, 2003 Amendment incorporated herein by reference.

First, Maa et al. clearly fails to teach or suggest "*a ... metal containing silicon was deposited to form the silicide*", as admitted by the Examiner.

Independent claims 1, 4, 13, 25, and 26 each clearly require a "metal containing silicon." (emphasis Applicant's), and claim 10 requires the metal be co-deposited with silicon. Maa does not teach or suggest the use of a metal-silicon alloy as silicidation material. Indeed, Maa teaches away from such a claimed feature.

As mentioned previously, Maa defines a "silicidation material" as one of pure metals such as "Co, Ti, Ni, W, Pt, Pd, Mo and Ta" (e.g., see Col. 4, line 63 of Maa). Maa suggests the use of a multi-layer stack "*[l]ayer 80 is either a uniform layer of a single metal, for example cobalt, or alternatively, is made up of more than one layer of silicidation material. For example, layer 80 might include a lower layer of Ti and upper layer of Co.*" (e.g., see Col. 4, line 64 to Col. 5, line 1 of Maa et al.).

In this regard, Maa does not even teach a metal alloy, let alone the use of a metal containing silicon or a metal co-deposited with silicon. In fact, Maa does not propose, teach, or suggest the use of any metal-silicon mixtures or metal-silicon alloys, but rather clearly teaches that a layered structure of pure metals is desirable.

Hence, Maa defines a "silicidation material" as one of pure metals such as "Co, Ti, Ni, W, Pt, Pd, Mo and Ta" (e.g., see Col. 4, line 63 of Maa). Maa suggests the use of a multi-layer stack "*[l]ayer 80 is either a uniform layer of a single metal, for example cobalt, or alternatively, is made up of more than one layer of silicidation material. For example, layer 80 might include a lower layer of Ti and upper layer of Co.*" (e.g., see Col. 4, line 64 to Col. 5, line 1 of Maa et al.). Hence, Maa teaches only silicidation materials as being pure metals (i.e., refractory metals or noble metals), and with each being formed as a layer. There is no teaching or suggestion of a metal alloy, let alone "a metal containing silicon", as in the claimed invention.

To make up for the deficiencies of Maa, the Examiner relies on Cabral et al. '131 and refers to the Abstract and to column 6, lines 4-16 of Cabral et al. '131.

However, Cabral fails to do so. Cabral teaches a method for solving a problem completely unlike that of Maa et al., let alone that of the present invention, and thus it comes as no surprise that Cabral offers a much different method/solution (and focus) than that of Maa et al. Thus, the motivation for combining Cabral with Maa et al. is suspect and appears to have resulted mainly from the Examiner's keyword search after reading the present specification.

In any event, Cabral et al. does not make up for the deficiencies of Maa et al. Cabral et al. addresses the issue of the high temperature anneal required to form a low resistivity C54 phase, and proposes a method for lowering the formation temperature. It is noted that this issue is rather specific to titanium silicide, and does not apply to all silicides in general. Additionally, it is irrelevant to the claimed invention.

$TiSi_2$ phase can exist in two polycrystalline structures. The first polycrystalline structure (e.g., the C49 phase) has a resistivity of about 60-90 micro-ohm-cm.

The second polycrystalline structure (e.g., the C54 phase) has a lower resistivity of about 12-20 micro-ohm-cm, and is therefore the desired phase. The C49 phase forms at about 650 °C. The C54 phase forms at a higher temperature of about 766 °C (See Fig 12 in Cabral). However, such a high formation temperature can lead to device degradation, and agglomeration of the silicide film if a high enough anneal temperature is used to ensure the phase transformation for small circuit features.

Hence, Cabral et al. addresses the issue of the high temperature anneal required to form the low resistivity C54 phase, and proposes a method for lowering the formation temperature. As evident, this issue is rather specific to titanium silicide and does not apply to all silicides in general.

Specifically, Cabral proposes depositing a Ti film over a refractory metal such as Ta, Nb, Mo, or W, and annealing to form a C54 $TiSi_2$ phase. In a different embodiment, Cabral deposits a Ti-Si alloy over the refractory metal. This alloy is targeted to be stoichiometric $TiSi_2$, but may be richer or leaner in its silicon composition (See column 6, lines 4-17).

First, Applicant submits that, given the disparate problems faced by each of Maa, Cabral and the present invention, it would not have made it "obvious" to combine the references, absent impermissible hindsight construction of the present invention, made possible only through a keyword search by the Examiner after a thorough reading of Applicant's own specification. Cabral attempts to solve a much different problem than Maa (let alone that addressed by the

present invention as explained below), and specifically is concerned with a last forming phase of titanium silicide (i.e., the C54 phase), not a first forming phase of silicide as in the invention.

Secondly, Cabral is not proposing a process which reduces silicon consumption. Cabral's proposes a method for forming the C54-$TiSi_2$ at a lower temperature than the conventional method, and preferably with one anneal. One of ordinary skill in the art taking Maa et al. and recognizing its deficiencies, would not have looked to Cabral, absent impermissible hindsight.

Cabral is silent with respect to forming any of the intermediate silicon-rich phases. When annealing Ti over silicon, the following phases form with increased temperature:

Ti -> Ti_3Si -> Ti_5Si_3 -> Ti_5Si_4 -> TiSi -> C49-$TiSi_2$ -> C54-$TiSi_2$.

In contrast to Cabral, following the method of the present invention, one would first form a silicon-rich phase, such as the Ti_5Si_3 phase, etch the unreacted Ti, apply a silicon cap, and then run a second anneal to form the C54-$TiSi_2$ phase.

Cabral does not teach or suggest forming the Ti_5Si_3 phase or any other intermediate phase, but actually proposes a method that forms the final phase C54-$TiSi_2$ in one annealing step (e.g., a single annealing). This method is completely different from Maa et al., let alone the claimed invention. Indeed, Cabral attempts to avoid the second "conversion-anneal". His process will preferably have only one anneal step that will form the C54 $TiSi_2$ phase (See for example, column 2, lines 23-30, and column 6, lines 22-26).

Additionally, the embodiment in which Cabral proposes using a near stoichiometric $TiSi_2$ alloy, cannot be applied to the self-aligned silicide (SALICIDE) method. The SALICIDE process includes applying a blanket metal film (such as Ti) onto a device structure (such as a

MOSFET), annealing the wafer to react the metal with silicon surfaces to form a silicide (the metal over insulator surfaces, such as the MOSFET's sidewalls, does not convert into a silicide and remains a metal), etching the unreacted metal, and performing a second anneal to reach the desired silicide phase.

The above-described process is summarized in Cabral on column 1, line 47-55, and on column 11, line 48 to column 12, line 18. The etching is selective in the sense that it attacks the pure metal, but does not attack the silicide.

The salicide process cannot be performed with a blanket deposited Ti - Silicon alloy (as opposed to Ti alloy, which is defined in Cabral as Ti with some refractory metal) having a composition of stoichiometric $TiSi_2$, since the selective etch would no longer work. When a pure Ti or metallic Ti alloy is used, the metal over the device spacers does not convert into silicide during the anneal. Therefore, the unreacted metal can be etched since the etchant attacks only the metal, and does not remove silicide.

In contrast, when a near stoichiometric Ti-Silicon alloy is blanket deposited, the spacers are covered with a Ti silicide the same as the rest of the device surfaces and the selectivity of metal versus silicide is lost.

It is noted that this is precisely one of the reasons that Cabral specifies the refractive metal for forming the Ti alloy as being "preferably a metal that is capable of forming a metal silicide" (column 3, lines 65-66). In addition, Cabral describes the application of his invention to the SALICIDE method only with Ti alloy (column 11, lines 48-65).

Cabral "skips" the intermediate silicide phases. In contrast, Applicants are using a metal-semiconductor alloy to extend the temperature window in which the silicide metal-rich phase exists (the first silicide phase).

For example, this temperature window is extended from 20 °C to over 100 °C in the case of Co_2Si. This allows the invention to reliably form the metal-rich phase and apply the silicon cap as early as possible in the salicide process, thereby to reduce the silicon consumption. In complete and fundamental contrast, Cabral is trying to minimize the temperature window where the metal-rich silicide exists, so that the final phase (C54-$TiSi_2$) will form at a lower temperature than that of the conventional method. This is irrelevant to Maa et al., let alone teaches away from the claimed invention.

The only relevance (arguendo) that Cabral may have is that Cabral mentions the use of a metal and silicon for the purpose which Cabral is trying to achieve (i.e., minimize the temperature window). However, such a mention by Cabral has no connection or relevance to the purpose of the invention (reducing silicon consumption as early as possible in the silicide forming phases).

In sum, as described in the present application, the invention uses a very specific combination of steps employing a metal containing silicon or a metal co-deposited with silicon purposely and affirmatively to achieve its advantages, including widening the temperature window at which, for example, the Co_2Si (the first forming phase) is formed, thereby allowing application of the silicon cap at a very early stage (phase) that what Maa can do. Further, in the invention, there is some semiconductor material (e.g., silicon) in the deposited metal, thereby to

reduce the silicon consumption from the device substrate. Such are not reasonably achieved, taught or suggested by Maa and/or Cabral.

Thus, Applicants submit that Maa and Cabral would not have been combined by one of ordinary skill in the art at the time of the invention and absent hindsight.

Additionally, even assuming arguendo that Maa and Cabral would have been combined in the manner urged, the claimed invention would still not have been produced. That is, there is no teaching or suggestion of the metal containing silicon or the metal co-deposited with silicon to form the silicide for a device. Thus, claims 1, 4, 10, 13, 25, and 26 are patentable over the Examiner's proposed combination.

Regarding dependent claims 2, 3, 5, 6, 8, 12, 23, 24, 27-30, and 33-38, these claims are patentable not only by virtue of their dependency from the above independent claims, but also for the additional limitations which they recite.

That is, first, with regard to dependent claims 23 and 24, Maa does not teach the use of a first forming phase as in the claimed invention. The Examiner indicates that the first silicide phase is the first forming silicide phase. This is not necessarily the case as a review of Maa et al. and Cabral would indicate.

Maa admits, in the disclosure thereof, that "*the compound form in 90 in Fig. 5 may contain both Co_2Si and CoSi*" (col. 5, line 30), with the reason being the narrow temperature window in which this first forming phase exists. This is precisely why Maa's disclosure avoids the term "metal-rich phase" when referring to 90 and instead named 90 as a "silicon deficient silicide".

Even assuming arguendo that Maa realized that it is preferable to form Co_2Si rather than CoSi to reduce silicon consumption from the substrate (Col. 5, lines 49-52), Maa only discusses the "likelihood of forming Co_2Si being improved if the temperature range is between 450C to 500C" (Col. 5, lines 55-57). However, Maa provides no sound method by which only Co_2Si is obtained from such a process. Indeed, Maa avoids the term "metal-rich phase" and uses the term "silicon deficient silicide".

Thus, Maa merely mentions that Co_2Si may be preferable, but teaches or suggests no method of getting there, and certainly not with the clear, unique, and unobvious combination of process steps of the present invention.

Maa teaches no method for obtaining Co_2Si. He merely discloses that there may be an incidental chance of obtaining Co2Si (presumably if many hundreds (or thousands) of wafers are processed) and that such would be preferable over CoSi. Again, there is no description, disclosure or suggestion of how to form the Co_2Si phase.

Maa, in discussing formation of the first phase (CoSi), discloses that it may be a mixture of CoSi and Co_2Si, because Maa has no way to control what phase will form. A reason why the industry has not used the Co_2Si phase, is because it has a very narrow temperature formation window.

In contrast, the invention provides a clear, reliable method of producing (e.g., how to get to) the second phase (Co_2Si), and then forms a silicon cap thereover for the purpose of reducing silicon consumption, as discussed above.

In complete and fundamental contrast, the claimed invention has clear process steps utilizing a metal containing silicon as a way to obtain, for example, Co_2Si (and as defined in claims 23 and 24, etc. as the "first forming phase"). Moreover, the incorporation of silicon into the metal reduces further the silicon consumption from the wafer already at the formation of the Co_2Si phase. None of these exemplary features is taught or suggested by Maa and/or Cabral et al.

Additionally and for the record, regarding dependent claims 28, 30, 34, 36, and 38, the Examiner asserts again on page 4 of the Office Action that "*[r]egarding claims 28, 30, 34, 36, and 38 it is seen to be inherent that the metal-alloy extends the temperature window in which a silicide metal-rich phase exist ... In other words, the more metal that is present relative to silicon the longer the window. Consequently if an alloy absent silicon is used the window is larger then if silicon is present.*"

However, the Examiner's statement is not understood. Indeed, Applicant emphasizes that this is erroneous. In fact, it just the opposite.

Page 16, lines 3-8 of the specification disclose that "*[t]he temperature window for Co_2Si is about 20°C wide if pure Co is used. It may be widened to about 100°C by using $Co_{0.8}Si_{0.2}$. The window may shift and vary depending on the SOI doping. This makes it difficult to obtain the Co_2Si phase if the window is narrow. If pure Co rather than $Co_{0.8}Si_{0.2}$ is used, then it is easier to form CoSi due to its large temperature window of about 150°C.*" (emphasis ours)

That is, with regard to the metal-rich phase (e.g., Co_2Si) the addition of silicon to the metal widens the temperature window. Thus, the Examiner's statement on page 4 of the Office Action that "in other words, the more metal that is present relative to silicon, the longer the

window", is clearly incorrect. Indeed, it is just the opposite. Adding silicon widens the window, not shortens it.

Referring to the exemplary case of cobalt-silicon alloy, an alloy absent of silicon results in a window that is only 20 °C wide. That is, in stoichiometric analysis, the metal (e.g., cobalt) would have a value of 1.0 and the silicon would have a value of 0, since it is not present. However, with the addition of 20% silicon, thus forming a Co(0.8)- Si(0.2) alloy, the window opens up and is 100°C wide. This is a major benefit of the invention, and is not at all appreciated by Maa. It is noted that the window being referred to is in the Co_2Si phase, not necessarily the CoSi phase mentioned in lines 7-8 of page 16.

Therefore, the use of a metal containing silicon is important for obtaining the first forming phase Co_2Si. Such is not taught or suggested anywhere within Maa et al.

It is noted again that since the Co_2Si phase only exists in a very narrow, tight temperature window, it is very difficult to form (e.g., very unreliable and prone to error or being missed based on nonuniform doping of the substrate, etc.) and control, as noted above, and, in practice, the later phase (e.g., CoSi) is typically used in self-aligned silicide processes.

The Examiner is again respectfully referred to Figures 2A and 2B of Exhibit I submitted with the Amendment of May 14, 2002.

The bottom map (e.g., Figure 2B) shows the evolution of reacting a metal (e.g., Co) containing silicon, as in the claimed invention. That is, Figure 2B shows the metal (e.g., Co)-silicide phases when a Co-silicon mixture having 20% silicon is used instead of pure Co. In this case, the Co_2Si phase exists over a large temperature window of more than 100 °C. This

makes it possible to practice a self-aligned silicide process where the first phase is also the first forming phase (Co_2Si), as defined in some of the dependent claims (e.g., 23, 24, etc.).

As a result, a much more reliable and easier manufacturing process is possible since it is easier to stop on Co_2Si, etc. Hence, the invention allows much greater control in forming the Co_2Si, as described above. Then, annealing can be performed, etc. to go to CoSi, and finally to $CoSi_2$. Such is not trivial to use the method above (including using the metal-silicon mixture), and thus, it is clear that Cabral et al. does not make up for the deficiencies of Maa. Thus, Applicants submit that Maa and Cabral would not have been combined by one of ordinary skill in the art at the time of the invention and absent hindsight.

Additionally, even assuming arguendo that Maa and Cabral would have been combined in the manner urged, the claimed invention would still not have been produced. Thus, claims 10 and 31-32 are patentable over the Examiner's proposed combination.

IV. THE DOUBLE PATENTING REJECTIONS

With respect to the double patenting rejections, claims 1, 4, 10, 25, and 26, stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 28-31 of Ajmera et al. (U.S. Patent No. 6,503,833 B1).

However, Applicant has again closely reviewed claims 24 and 28-31 of Ajmera, et al., and submits that there is no teaching or suggestion by these claims of "*depositing a metal containing silicon on a silicon substrate*", as in claim 1 and substantially similarly in independent claims 4, 10, 25, and 26.

Further, there is no teaching or suggestion of "*reacting said metal containing silicon to form a first silicide phase*" (emphasis Applicant's), as defined by independent claim 1, and similarly by claim 4, 10, 25, and 26. Such a limitation is clearly not found or suggested in any of claims 24 and 28-31 of Ajmera

Hence, there are clear limitations found in claims 1, 4, 10, 25, and 26 which are not taught or suggested by claims 24 and 28-31 of Ajmera.

Claims 1 and 27 of Cabral, Jr., et al., '578 B1 are similarly deficient.

Finally, regarding the provisional double patenting rejections, the Examiner indicates that claims 1, 4, 10, 25, and 26 conflict with: claims 24 and 28-31 of Application No. 10/287,476; claims 1, 4, 5, and 23 of Application No. 10/299,688; and claims 15 and 20 of copending Application No. 09/902,483.

However, the claims of these copending applications have been reviewed and clearly do not conflict, teach, or suggest all of the subject matter of the present claims. Indeed, different inventions are being prosecuted and specifically methods directed to different inventive steps.

Again, there is no teaching of suggestion by these claims of "*depositing a metal containing silicon on a silicon substrate;*

reacting said metal containing silicon to form a first silicide phase;

etching any unreacted metal containing silicon..." (Emphasis Applicant's), as in claim 1 and substantially similarly in independent claims 4, 13, 25, and 26. Again, for a double patenting rejection, only the claims of the applied patent can be relied upon, not the disclosure. Thus, here there are limitations in claims 1, 4, 10, 24, and 26 which are not taught or suggested by any of the

claims of the copending applications. Thus, the claims of the present application do not conflict with, taught or suggested by any of the claims of the copending application Nos. 10/287,476, 10/299,688, or 09/569,306.

Notwithstanding the above, Applicant reserves the opportunity to file a Terminal Disclaimer at a later time, once the prior art rejection is overcome.

In view of all of the foregoing, Applicant submits that all of the pending claims are patentable over the prior art of record.

V. FORMAL MATTERS AND CONCLUSION

Claims 8 and 26 have been amended to overcome the Examiner's objections thereto.

In view of the foregoing, Applicant submits that claims 1-8, 10-13 and 23-38, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 5/13/04

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this paper via facsimile, to Group Art Unit 2813, at (703) 872-9306, on May 13, 2004.

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